Office Action Summary	Application No.	Applicant(s)	
	10/775,523	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20080404* .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's submission of the Appeal Brief filed on January 11, 2008 is acknowledged. Applicant's remarks submitted in the Appeal Brief are considered persuasive. In view of the Appeal Brief filed on January 11, 2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Therefore the FINALITY of the office action dated August 10, 2007 is hereby withdrawn. The examiner requests the applicants to consider the new grounds of rejection provided below. Currently, claims 1-20 are pending for examination.

I. OBJECTION TO ABSTRACT

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the abstract disclosure is insufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See MPEP § 608.01(b).

II. OBJECTION TO THE CLAIMS

5. Claims 6 and 9 are objected to because of the following informalities:

in claim 6, line 1, "said first, second and third ports" should be replace with -said first, second and third SATA ports-.

in claim 9, line 3, "said first ATA port" should be replace with -said first SATA port-.

Appropriate correction is required.

III. REJECTIONS 35 U.S.C. 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 9, 14 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, in line 16, it is not fully clear to the examiner if the claimed limitation should be "and" or "or;" the examiner will assume the claimed limitation of "or for the current examination.

As per claim 9, in line 20, it is not fully clear to the examiner if the claimed limitation should be "and" or "or;" the examiner will assume the claimed limitation of "or for the current examination.

As per claim 14, in line 20, it is not fully clear to the examiner if the claimed limitation should be "and" or "or;" the examiner will assume the claimed limitation of "or for the current examination.

As per claim 19, in line 20, it is not fully clear to the examiner if the claimed limitation should be "and" or "or;" the examiner will assume the claimed limitation of "or for the current examination.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-7 and 9-20 are rejected under 35 U.S.C. 103(a) as being anticipated by Grieff et al. (US Patent 6,961,813) in view of Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787).

8. As per claims 1, 9 and 14, Grieff teaches a switch coupled between a plurality of host units and a device via serial advanced technology attachment (SATA) links, for routing frame information there between the first and the second host units and the device, said switch comprising:

a. a first SATA port (H0_Link Layer 130 of Fig. 1) for connecting to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

b. a second SATA port (H1_Link Layer 132 of Fig. 1) for connecting to a second host unit responsive to a non-data FIS from the second host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

c. a third SATA port (Device-Side Link Layer of Fig. 1), responsive to a non-data FIS, coupled to a device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

d. an arbitration and control circuit (switch 110 and arbiter module 112 of Fig. 1) for selecting one of the first host or second host units to be coupled to the device, through the switch, and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive (col. 2, l. 53 to col. 3, l. 45;

col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56; col. 10, ll. 27-64 and col. 12, ll. 23-27);

wherein the switch enable multiple host units to share access to the device (e.g. single ATA device) (col. 3, ll. 14-16), such that the device can maintain communication with the multiple host units (col. 3, ll. 43-45); and

wherein the switch includes a buffer that allows the first host to post a single, non-queue command if the second host currently has outstanding queued commands (col. 5, ll. 36-39).

Grieff does not expressly teach the switch coupled between the plurality of host units and the device via SATA links, for routing frame information there between the first and the second host units and the device, said switch comprising:

wherein the first SATA port includes a first host task file;

wherein the second SATA port includes a second host task file;

selecting one of the first host or the second host units to concurrently access the device by accepting non-data FIS, from either of the first or the second host units, at any given time, including when the deice is not in an idle state; and

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the non-data FIS to the switch for routing to the device.

Utsunomiya teaches a system and a method comprising:

a host computer issuing a plurality of commands to the drive apparatus (Fig. 3, ref. 12) at the same time (e.g. concurrently), wherein the drive apparatus operates in accordance to ATA ([0004] and [0007]);

a command queue including a task file queue enabling the host computer to issue the plurality of commands to be processed by the drive apparatus at the same time (e.g. concurrently), as the task file queue storing the plurality of commands ([0005]-[0008] and [0020]-[0024]), therefore the task file queue would enable the host computer to issue the plurality of commands, at any given time, even when the drive apparatus is in a busy status ([0005]); and

wherein the plurality of commands issued by the host computer are transferred from the task file queue to the drive apparatus' task file (Fig. 5 and [0022]).

Ooi ('045) teaches a system and a method comprising a SATA port (Fig. 2, ref. 220, 230) having a serial port task file (Fig. 2, ref. 225, 235) (col. 3, l. 56 to col. 5, l. 15).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya and Ooi's task file queue into Grieff's ATA ports for the benefit of decreasing the work load of the host unit for issuing commands (Utsunomiya, [0009]) and provide backward compatibility between SATA and PATA (Ooi ('045), col. 1, ll. 13-42); additionally, the combining of the above references would be motivated because it is well known to one skilled in the art for ATA that SATA specification provides for systems having forward and backward compatibility with PATA as well as scalability and evolutionary enhancement to various types of

computing platforms and chipsets in computer systems (Ooi ('787), col. 1, ll. 13-42). The resulting combination of the references further teaches the switch comprising:

wherein the first SATA port includes the first task file queue (i.e. first host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the first host unit;

wherein the second SATA port includes the second task file queue (i.e. second host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the second host unit; and

wherein the switch selects either the first host unit or the second host unit to concurrently access the drive apparatus (i.e. device) as the switch receives and accepts the plurality of commands (i.e. non-data FIS), issued by either the first host unit or the second host unit, at any give time, including when the device is in the busy status (i.e. not in an idle state), as the plurality of commands are respectively stored into the first task file queue and the second task file queue; therefore, as one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the command (i.e. non-data FIS) to the switch, stored by the respective task file queue, for routing to the device apparatus.

9. As per claims 2, 11 and 16, Grieff, Utsunomiya and Ooi teach all the limitations of claims 1, 9 and 14 as discussed above, where Grieff further teaches said switch comprising wherein said device is a storage unit (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 15, ll. 9-22).

10. As per claims 3, 12 and 17, Grieff, Utsunomiya and Ooi teach all the limitations of claims 1, 9 and 14 as discussed above, where Grieff further teaches said switch comprising wherein said switch is employed in an enterprise system (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 15, ll. 9-22).

11. As per claims 4, 13 and 18, Grieff, Utsunomiya and Ooi teach all the limitations of claims 1, 9 and 14 as discussed above, where Utsunomiya further teaches said switch comprising wherein said arbitration and control causes concurrent access of the device by the first and the second host units (Utsunomiya, Fig. 4-5).

12. As per claim 5, Grieff, Utsunomiya and Ooi teach all the limitations of claim 1 as discussed above, where Grieff further teaches said switch comprising wherein a bit is used to indicate which host is the origin or destination of the non-data FIS (Grieff, col. 4, ll. 47-57 and col. 10, l. 27 to col. 12, l. 29), as each non-data FIS comprise an associated 5-bit tag utilized for identifying which host is the origin or the destination of the FIS.

13. As per claim 6, Grieff, Utsunomiya and Ooi teach all the limitations of claim 1 as discussed above, where Grieff further teaches said switch comprising wherein said first, second and third SATA ports are layer 2 ports (link layer ports) (Grieff, Fig. 1).

14. As per claims 7 and 10, Grieff, Utsunomiya and Ooi teach all the limitations of claims 1 and 9 as discussed above, where Grieff further teaches said switch comprising wherein the switch provides for `route aware` routing (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56 and col. 12, l. 60 to col. 14, l. 21), as FIS are properly routed between one of the associated hosts and the device.

15. As per claim 15, Grieff, Utsunomiya and Ooi teach all the limitations of claim 14 as discussed above, where Grieff further teaches said switch comprising wherein the switch is a serial ATA switch (Grieff, col. 5, ll. 17-21).

16. As per claim 19, Grieff teaches a method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween, comprising:

a. receiving a non-data frame information structure (FIS) through a first serial ATA (SATA) port (H0_Link Layer 130 of Fig. 1), from to a first host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

b. receiving a non-data FIS, through a second SATA port (H1_Link Layer 132 of Fig. 1), from a second host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

c. receiving a non-data FIS through a third SATA port (Disk-Side Link Layer of Fig 1) (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

d. arbitrating (arbitrate utilizing the arbiter module 112 of Fig. 1) between the first and second host units and the device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends request for execution by the device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

f. coupling the device to the selected one of the first or second host units (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56); and

the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56; col. 10, ll. 27-64 and col. 12, ll. 23-27).

Grieff does not teach the method for communication between multiple host units and the device comprising:

while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device.

Utsunomiya teaches a system and a method comprising:

a host computer issuing a plurality of commands to the drive apparatus (Fig. 3, ref. 12) at the same time (e.g. concurrently), wherein the drive apparatus operates in accordance to ATA ([0004] and [0007]);

a command queue including a task file queue enabling the host computer to issue the plurality of commands to be processed by the drive apparatus at the same time (e.g. concurrently), as the task file queue storing the plurality of commands ([0005]-[0008] and [0020]-[0024]), therefore the task file queue would enable the host computer to issue the plurality of commands, at any given time, even when the drive apparatus is in a busy status ([0005]); and

wherein the plurality of commands issued by the host computer are transferred from the task file queue to the drive apparatus' task file (Fig. 5 and [0022]).

Ooi ('045) teaches a system and a method comprising a SATA port (Fig. 2, ref. 220, 230) having a serial port task file (Fig. 2, ref. 225, 235) (col. 3, l. 56 to col. 5, l. 15).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya and Ooi's task file queue into Grieff's ATA ports for the benefit of decreasing the work load of the host unit for issuing commands (Utsunomiya, [0009]) and provide backward compatibility between SATA and PATA (Ooi ('045), col. 1, ll. 13-42); additionally, the combining of the above references would be motivated because it is well known to one skilled in the art for ATA that SATA specification provides for systems having forward and backward compatibility with PATA as well as scalability and evolutionary enhancement to various types of

computing platforms and chipsets in computer systems (Ooi ('787), col. 1, ll. 13-42). The resulting combination of the references further teaches the switch comprising:

wherein the first SATA port includes the first task file queue (i.e. first host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the first host unit;

wherein the second SATA port includes the second task file queue (i.e. second host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the second host unit;

wherein the switch selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device; and

wherein the switch selects either the first host unit or the second host unit to concurrently access the drive apparatus (i.e. device) as the switch receives and accepts the plurality of commands (i.e. non-data FIS), issued by either the first host unit or the second host unit, at any give time, including when the device is in the busy status (i.e. not in an idle state), as the plurality of commands are respectively stored into the first task file queue and the second task file queue; therefore, while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the command (i.e. non-data FIS) to the switch, stored by the respective task file queue, for routing to the device apparatus.

17. As per claim 20, Grieff, Utsunomiya and Ooi teach all the limitations of claim 19 as discussed above, where Grieff further teaches the method comprising wherein the steps of transmitting a non-data FIS through the first SATA port, through the second SATA port, and transmitting a non-data FIS through the third SATA port (Grieff, col. 4, ll. 5-34 and col. 10, l. 27 to col. 12, l. 29), wherein the non-data FIS is transmitted from the host-side through either the first or the second serial ATA ports and from the device through the third serial ATA port.

18. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) and Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi (US Patent 6,961,787) as applied to claim 1, and further in view of Kreifels (US Patent 4,891,788).

Grieff, Utsunomiya and Ooi teach all the limitations of claim 1 as discussed above, but do not expressly teach said switch comprising a dual ported first-in-first-out (FIFO).

Kreifels teaches a system and a method comprising a dual port FIFO (Fig. 1).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels' dual port FIFO into Grieff, Utsunomiya and Ooi's switch's inbound buffers for the benefit of enabling the read and write operation of the inbound buffer to be independent of each other (Kreifels, col. 1, l. 15 to col. 2, l. 6). The resulting combination of the references teaches the switch further comprising the utilization of dual port FIFO.

II. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 07, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181